

**WHAT IS CLAIMED IS:**

1. A method of forming a semiconductor device comprising:  
forming field regions in a substrate to define a first transistor  
5 region, a capacitor region, and a second transistor region;  
forming a first gate stack in the first transistor region and a lower  
electrode in the capacitor region; and  
forming an upper electrode on the lower electrode with a  
dielectric layer interposed therebetween and a second gate stack in the  
10 second transistor region.

2. The method of claim 1, wherein forming the first gate  
stack and the lower electrode comprises:  
forming a first insulation layer and a first conductive layer on the  
15 substrate; and  
patterning the first conductive layer and the first insulation layer  
to form the first gate stack and the lower electrode, and  
wherein forming the upper electrode with dielectric layer  
interposed thereunder and the second gate stack comprises:  
20 forming a dielectric layer on the lower electrode;  
forming a second insulation layer and a second conductive layer;  
and  
patterning the second conductive layer and the second insulation  
layer to form the upper electrode and the second gate stack.

25 3. The method of claim 2, wherein the first insulation layer  
and the second insulation layer are formed having different thicknesses  
from each other.

4. The method of claim 1, wherein forming the first gate stack and the lower electrode comprises:

forming a first insulation layer, a first conductive layer, and a dielectric layer on the substrate; and

5 patterning the dielectric layer, the first conductive layer and the first insulation layer to form the first gate stack, the lower electrode and the dielectric layer, and

wherein said step of forming the upper electrode and the second gate stack comprises:

10 forming a second insulation layer and a second conductive layer on the substrate; and

patterning the second conductive layer and the second insulation layer to form the upper electrode and the second gate stack.

15 5. The method of claim 4, wherein the first insulation layer and the second insulation layer are formed having different thicknesses from each other.

20 6. The method of claim 1, wherein the dielectric layer is a material selected from the group consisting of silicon oxide, silicon nitride, oxide-nitride-oxide, tantalum oxide, barium-strontium-titanium oxide, zirconium oxide, hafnium oxide, plumbum-zinc-titanium oxide, strontium-bismuth-tantalum oxide, and any combination thereof.

25 7. A method of forming a semiconductor device comprising:  
forming field regions in a substrate to define a first transistor region, a capacitor region, and a second transistor region;  
forming a gate pattern in the first transistor region and a lower electrode in the capacitor region;

forming an upper electrode with a dielectric layer interposed between the upper electrode and the lower electrode and a second gate stack in the second transistor region; and

5 patterning the gate pattern to form a first gate stack in the first transistor region.

8. The method of claim 7, wherein forming the gate pattern and the lower electrode comprises:

10 forming a first insulation layer and a first conductive layer on the substrate; and

patterning the first conductive layer and the first insulation layer to form the first gate pattern and the lower electrode, and

wherein forming the upper electrode with the dielectric layer interposed thereunder and the second gate stack comprises:

15 forming a dielectric layer on the lower electrode;

forming a second insulation layer and a second conductive layer; and

patterning the second conductive layer and the second insulation layer to form the upper electrode and the second gate stack.

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9. The method of claim 8, wherein the first insulation layer and the second insulation layer are formed having a different thickness from each other.

25 10. The method of claim 7, wherein forming the gate pattern and the lower electrode comprises:

forming a first insulation layer, a first conductive layer and a dielectric layer on the substrate; and

patterning the dielectric layer, the first conductive layer and the

first insulation layer to form the gate pattern, the lower electrode and the dielectric layer, and

wherein said step of forming the upper electrode and the second gate stack comprises:

5           forming a second insulation layer and a second conductive layer on the substrate; and

          patterning the second conductive layer and the second insulation layer to form the upper electrode and the second gate stack.

10           11.     The method of claim 10, wherein the first insulation layer and the second insulation layer are formed having a different thickness from each other.

15           12.     The method of claim 7, wherein edges of the gate pattern formed in the first transistor region overlap the field regions.

          13.     The method of claim 7, wherein the dielectric layer is a material selected from the group consisting of silicon oxide, silicon nitride, oxide-nitride-oxide, tantalum oxide, barium-strontium-titanium oxide, zirconium oxide, hafnium oxide, plumbum-zinc-titanium oxide,  
20           strontium-bismuth-tantalum oxide, and any combination thereof.

          14.     A method of forming a semiconductor device comprising:  
          (a) forming isolation layers in predetermined regions of a  
25           semiconductor substrate to define a first region, a second region and a third region;

          (b) forming a first gate insulating layer and a first gate conductive pattern stacked sequentially on the first region, a second gate insulating layer and a second gate conductive pattern stacked

sequentially on the second region, and a third gate insulating layer and the second gate conductive pattern stacked sequentially on the third region; and

(c) patterning together the first gate conductive pattern and the second gate conductive pattern to form a first gate electrode, a second gate electrode and a third gate electrode in the first, second and third regions, respectively,

wherein the first gate insulating layer, the second gate insulating layer and the third insulating layer are formed having varying thicknesses and each layer has a different thickness than the other layers.

15. The method of claim 14, wherein the (b) step comprises:  
forming the first gate insulating layer and the first gate conductive pattern stacked sequentially on the first region;  
forming a second gate conductive layer on the entire surface of the semiconductor substrate having the second and third gate insulating layers; and

patterning the second gate conductive layer to form the second gate conductive pattern exposing the first gate conductive pattern in the first region.

16. The method of claim 15, wherein forming the first gate insulating layer and the first gate conductive pattern comprises:  
forming the first gate insulating layer on the first region;  
forming a first gate conductive layer on the semiconductor substrate having the first gate insulating layer; and  
patterning the first gate conductive layer to form the first gate conductive pattern and a capacitor lower electrode, the first gate

conductive pattern is disposed in the first region and the capacitor lower electrode is disposed on a predetermined region of the isolation layers.

17. The method of claim 16, after patterning the first gate  
5 conductive layer, further comprising:  
forming a dielectric layer on the semiconductor substrate having  
the first gate conductive pattern and the capacitor lower electrode;  
patterning the dielectric layer to form a dielectric pattern, the  
dielectric pattern exposes the second and third regions and covers the  
10 first conductive pattern and the capacitor lower electrode.

18. The method of claim 17, wherein the dielectric layer is a  
material selected from the group consisting of silicon oxide, silicon  
nitride, oxide-nitride-oxide, tantalum oxide, barium-strontium-titanium  
15 oxide, zirconium oxide, hafnium oxide, plumbum-zinc-titanium oxide,  
strontium-bismuth-tantalum oxide, and any combination thereof.

19. The method of claim 17, further comprising forming an  
anti-reflecting layer on the second gate conductive layer, before  
20 patterning the second gate conductive layer,  
wherein forming the anti-reflecting layer comprises selecting a  
material and controlling a thickness of the selected material for the anti-  
reflecting layer to provide, in the step (c), the anti-reflecting layer  
having a non-selective etching characteristic with respect to the  
25 dielectric layer.

20. The method of claim 17, wherein forming the second gate  
conductive pattern comprises forming a capacitor upper electrode on the  
dielectric pattern opposite the capacitor lower electrode.

21. The method of claim 17, wherein the step (c) further comprises forming a capacitor upper electrode on the dielectric pattern opposite the capacitor lower electrode.

5 22. The method of claim 14, wherein the first gate conductive pattern and the second conductive pattern are formed of the same material.

10 23. The method of claim 22, wherein the first gate conductive pattern and the second conductive pattern are formed of polycrystalline silicon.

15 24. The method of claim 14, wherein the first gate insulating layer is silicon dioxide with a thickness of between about 50 Å to about 300 Å formed by thermal oxidation;

the second gate insulating layer is silicon dioxide with a thickness of between about 10 Å to about 100 Å formed by thermal oxidation; and

20 the third gate insulating layer is silicon dioxide with a thickness of between about 100 Å to about 1000 Å formed by a chemical vapor deposition.